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(30) Priority: 30.10.81 US 316573

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(71) Applicant: International Business Machines Corporation, Armonk, N.Y. 10504 (US)

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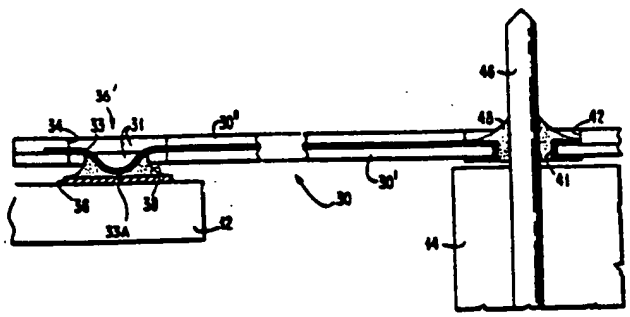

EP 0 080 041 A2

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 90 30 8151

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 32, no. 2, July 1989, pages 262-265, Armonk, NY, US; "Edge connected TAB memory package" * Whole article *	1-5, 11,12	H 01 L 23/498 H 01 L 23/057 H 01 L 23/538
Y	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 14, no. 10, March 1972, page 2911; B.R. KRYZANIWSKY: "Chip air cooling arrengement" * Whole article *	10,16	
Y	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 24, no. 2, July 1981, pages 1214-1215; L.V. AULETTA et al.: "Flexible tape conductor interconnection for chips" * Whole article *	10,16	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 01 L
A	US-A-3 780 352 (REDWANZ) * Abstract; figure 6; column 6, line 11 - column 7, line 47 *	6,10 16	
A	WO-A-87 06 766 (HONEYWELL) * Abstract; figures 1-3 *	6-9, 14,15	

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Place of search	Date of completion of the search	Examiner
THE HAGUE	26-02-1991	PROHASKA

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
P,X	GB-A-2 218 847 (GE) * Abstract; figure 2; page 2, last paragraph - page 3, third paragraph *	1,2,5 12-14	
P,A	WO-A-89 12 911 (UNISTRUCTURE) * Abstract; figures 2,2A *	6,10, 16	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions.

namely:

1. Claims 1-16: Device and method for connecting semiconductor die(s)(RAMs) to lead arrangement of package.

2. Claims 17,18: Testing, sorting method before assembly of packages to a board.

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid,

namely claims:

☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

namely claims: 1-16

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(88) Date of deferred publication of search report: **15.05.85 Bulletin 85/20**

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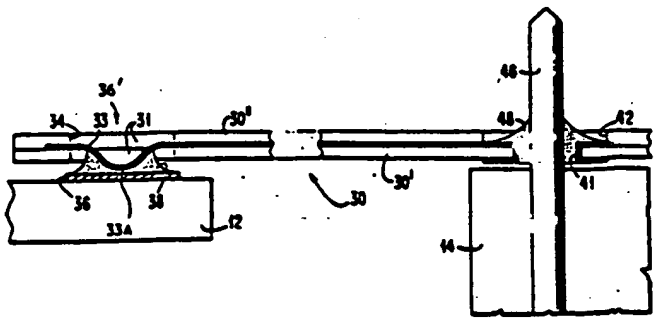

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INTER-CONNECTING DEVICES FOR ELECTRIC CIRCUITS

The invention relates to inter-connecting devices for electric circuits and is particularly concerned with interconnecting devices for connecting a wafer or substrate carrying electrical circuitry to connecting terminals of utilization circuitry.

It has sometimes been the practice to connect circuit terminals on a substrate carrying electrical circuitry to terminals connected to utilization circuitry by means of additional interconnecting members frequently referred to as packaging member assemblies.

Many packaging member assemblies and packaging members have been devised and improvements made. Cost reduction alone has spurred many such projects. Thermal relationships between components and/or the interconnecting packaging member have resulted in different structures. Power dissipation, other than that of thermal nature, wirability and "crossover" capability are other factors of interest. All of these factors have been considered and particular attention has been given to surer gang solderability and increased terminal density in the development of the packaging member according to the invention.

U. S. specification No. 4,231,154 (Gazdik) discloses a packaging member assembly including a device for individually inter-connecting contact pads formed on a semi-conductor chip or wafer and connecting pins to which external connections can be made. The device comprises a thin flexible printed circuit member providing an insulating sheet having a multiplicity of electrically separate conductors formed thereon. Each conductor extends from an associated one of a multiplicity of holes formed through the sheet and arranged in a pattern matching the locations of the pins to a multiplicity of pad positions arranged in a pattern matching the locations of the pads on the chip or wafer.

In practice it has been found that the thickness of the solder pads on the chip or wafer can vary and this can lead to problems in joining them to the conductors on the sheet. For example, if one pad is high it can deform the sheet with a risk that it will hold the sheet away from an adjacent pad. If the adjacent pad happens to be low, any solder joint made therewith could be constricted and have a high resistance or a solder path could be established between the pads.

It is an object of the present invention to provide an improved packaging member assembly or interconnecting device in which the foregoing difficulties are avoided or substantially reduced.

Accordingly the invention provides a device for individually inter-connecting contact pads formed on a semiconductor wafer or substrate and connected to circuitry on the wafer or substrate and connecting pins to which external electrical connections can be made, said device comprising an insulating sheet having a multiplicity of electrically separate conductors formed thereon, each conductor extending from an associated one of a multiplicity of holes formed through the sheet and arranged in a pattern matching the locations of the pins to a multiplicity of pad positions arranged in a pattern matching the locations of the pads on the wafer or substrate, characterised in that a second multiplicity of holes are formed through the sheet, said second holes being located at the pad positions and each being of a size to encompass a pad, and in that the conductors respectively extend across the second holes and thereby form individual compliant mountings for the pads of the wafer or substrate.

Hereinafter there is described as an example of the invention an electric circuit packaging member comprising a flat flexible film of annular configuration having apertures arranged near the inner and outer peripheries thereof overlapping the locations of substrate connecting pads and connecting block pins. Electronically conductive leads are arranged between corresponding apertures on the inner and outer peripheries. These leads preferably are formed by laminating conductive material, preferably

copper, to the entire film and etching to form conductive lands bridging the apertures corresponding to the connecting pads and preformed for soldering at the inner ends and apertured at the outer ends for surrounding the connecting pins. Preferably, the outer ends result in through plated viaducts for better soldering to the connecting pins. Solder fillets between the preformed lands at the one end and the pads tend to draw the bridging lands down onto the pads. The apertures in the film tend to confine the solder to the pad or pin located thereat and to prevent bridging to adjacent pads or pins.

Another film of substantially the same configuration is arranged over the lands for protection but has enlarged apertures for easier access for the soldering operation and acts as a solder slop.

The invention will now be further described with reference to the accompanying drawings, in which:-

FIG. 1 depicts a layout of components for electric interconnection by a carrier member embodying to the invention;

FIG. 2 is a plan view of an electronic circuit packaging interconnecting member embodying the invention;

FIG. 3 is a cross-section view of the interconnecting member taken along the line 3-3 in FIG. 2 and in relationship to a substrate terminal pad and a corresponding connector block pin;

FIG. 4 is a diagram showing the relative dimensions of parts of an electronic device assembly incorporating an interconnecting member embodying the invention; and

FIG. 5 is a diagram showing the configuration of parts at the connector pin end of a conductor of the electronic device assembly incorporating the interconnecting member embodying the invention.

A layout of electronic components requiring electronic interconnection is shown in FIG. 1 along with some detail of interconnection by a carrier member or device embodying the invention. A metal mounting base, preferably copper, 10 is arranged for supporting a substrate 12 and four connector blocks 14, 15, 16 and 17. The mounting base 10 is conventional in construction, as is the substrate 12 except for a staggered double row of terminal contact solder pads. The latter are arranged for the maximum number of pads possible in accordance with the feature of the invention that maximizes the number of Input/Output (I/O) leads in a given application. The connector blocks 14-17, likewise conventional, are chosen for one maximum density in an area convenient in size and shape for the application as will become more apparent as the specification progresses. A few semiconductor circuit chips 21-25 are shown by way of example only with but a few electric leads to I/O solder pads. Usually all, or nearly all, of the I/O pads are put to use; the usual problem is to work to the limited number available.

It remains in this illustration to provide electric connections individually between each I/O pad and a corresponding connecting pin on one of the four connector blocks. An interconnecting member 30 according to the invention is shown only generally by a pair of chain lines 32 and 34' in FIG. 1. This carrier member 30 is shown more clearly in FIGS. 2 and 3.

The interconnecting member 30 comprises at least a flexible polyimide film 30' and a multiple of electric current carrying conductors or lands 33. The member 30 is of generally annular configuration having an are (35) of similar but smaller size and shape to the chip or wafer 12. A protective covering of polyimide film 30" is provided to form a laminar structure. The two pieces of film are substantially identical except that the aperture 42 in the film 30" is larger than the aperture 41 in the film 30' at the connecting pin end of the conductor 33 as readily seen in FIG. 3; the apertures 31 are the same in both films 30' and 30", and the peripheral edges 32', 34' of the two films coincide at all points.

The contact apertures 31 and 41 (and 42) are made first. The conductors or lands 33 are then formed by laminating copper to the film 30' and etching according to a conventional process. The copper lands 33 in the pad contact apertures 34 are then bridged across the I/O pad apertures as shown. The lands 33 are depressed to the underside of the film 30', as shown, to form outwardly convex contacts 33A at the pad positions 36'. One method for so preforming comprises simple steps of placing a relatively flexible rubber sheet atop the upper film 30" and compressing this sandwich between rigid plates. The flow of rubber will form the loops in the aperture 31. The lands are formed about the connecting pin apertures 41 to form conductive viaducts as shown. The lands 33 and the I/O pads 36 are joined electrically by solder fillets 38. The preformed lands attract the solder due to surface tension and keep it from solder-bridging to other pads. These joints have some flexibility also. Solder fillets 48 electrically join the lands 33 to the pins 46.

FIGS. 4 and 5 are plan views about the apertures 31 and 41-42, respectively. From these views, it is readily seen that despite the high density of I/O pads 36 and connecting pins 46, there is sufficient room to accommodate some misalignment that inadvertently creeps into any manufacturing process.

This interconnective design effectively places substrate I/O lines close on centres by using two staggered rows of I/O pads on each side of the substrate as shown in FIG. 2. The spacing between I/O pads on the substrate 12 and on the member 30 is defined by the photolithographic techniques used. Spacing tolerance is controlled by the accuracy of the photolithographic technique, not by the physical dimensions of the ceramic substrate or those of the connector blocks.

The form factor of the copper land combined with the wetting action and surface tension of the solder will result in the formation of a solder joint as shown in FIG. 3.

This joint form factor provides a more compiant bond for each of the I/O pads.

The first design feature is that of an alignment aid. This is illustrated in FIGS. 4 and 5. By centering the copper land and contact aperture over the solder pad for contacts on opposite corners of the substrate, all contacts will be closely centred when joined. The second feature of the design is its deterrent to solder bridging between contacts and/or lines. The form factor of the contact will cause the solder to concentrate about the copper land during the gang soldering step of joining the interconnecting member 30 to the substrate.

The end of the copper land 33 bridging a contact aperture is extended sufficiently beyond the opening 31 to provide a secure anchoring of the land to the polyimide film. This serves to keep the copper lands in close registration with contact design centres. Space is provided between the inner edges of the member 30 and the contact apertures and similarly between the edges of the substrate to allow a conductor to go around one or more contacts. This provides an effective cross-over capability which enhances wirability.

In an exemplary embodiment of interconnecting members according to the invention, the substrate 12 was arranged with two staggered rows of I/O pads 36 around the periphery thereof. In one embodiment, a 36mm substrate was made with 63 I/O pads on each side. This effectively spaced the pads on 20 mil centres. The diameter of the contact in the polyimide film 30' was 28 mils. The width of the thin copper land bridging is 14 mils. The width of the solder pad on the ceramic substrate was 20 mils.

This design concept provides 252 I/O's on a 36mm substrate without serious impact on substrate area available for chips and wiring. Chip area available is about 3.05cm (1.2 inches) square or 68 percent of the surface area of a 36mm substrate. Use of this feature is illustrated schematically in FIG. 1. Five VLSI chips, about 6mm square, can be placed

comfortably within the mounting surface area available on a multilevel ceramic substrate.

The electronic circuit device packaging member hereinbefore described enables a higher density of substrate pads and connection block pins to be connected at lower cost and greater yield than for prior art devices. As described the packaging member comprises a multiple of conductors fixed in place by a flexible film carrier of annular configuration surrounding a ceramic substrate bearing electronic circuit components having input/output terminal connecting pads about the periphery of the substrate. Electric circuit connecting blocks having connecting pins are arranged at the periphery of the annular carrier. The multiple of conductors individually interconnect corresponding pads and pins. The film carrier has apertures at the locations of the pads and at the locations of the pins where the conductors or lands are configured for ready connection to the pads and pins, or by gang soldering. The dimensions and the arrangement of the apertures and the conductors or lands afford considerable leeway in making the connections.

CLAIMS

1. The device for individually inter-connecting contact pads formed on a semiconductor wafer or substrate and connected to circuitry on the wafer or substrate and connecting pins to which external electrical connections can be made, said device (30) comprising an insulating sheet (30') having a multiplicity of electrically separate conductors (33) formed thereon, each conductor (33) extending from an associated one of a multiplicity of holes (41) formed through the sheet (30') and arranged in a pattern matching the locations of the pins (46) to a multiplicity of pad positions (36') arranged in a pattern matching the locations of the pads (36) on the wafer or substrate (12), characterised in that a second multiplicity of holes (34) are formed through the sheet (30'), said second holes (34) being located at the pad positions (36') and each being of a size to encompass a pad (36), and in that the conductors (33) respectively extend across the second holes (34) and thereby form individual compliant mountings for the pads (36) of the wafer or substrate.

2. A device as claimed in claim 1, further characterised in that the sheet (30') has an aperture (35) therethrough of similar but smaller shape and size to the wafer or substrate (12) to be used therewith and in that the second holes (34) at the pad positions (36') are located in the margin of the sheet around the aperture (35).

3. A device as claimed in claim 2, further characterised in that the sheet (30') is of generally annular configurations, in that the first holes (42) at the pin locations are located in the margin of the sheet around the external periphery thereof.

4. A device as claimed in claim 1, 2 or 3, further characterised in that the portions of the conductors extending across the second holes (34) are each depressed into and through the respective aligned hole to form a smooth outwardly convex, contact (33A) projecting from the other end of the hole (34) to which a pad can be connected.

5. A device as claimed in any one of claims 1 to 4, further characterised in that the portion of each conductor (33) extending to a pin-receiving-hole (42) is integral with a conductive lining (41) through the pin hole.

6. A device as claimed in any one of claims 1 to 5, further characterised in that a second insulating sheet (30") of similar configuration to the first sheet (30') overlies the conductors (33) to form a laminar structure, the second sheet (30") being arranged to prevent or block solder flow between adjacent pads (36) and adjacent pins (46) during soldering of pads and pins to the device.

7. A device as claimed in any one of claims 1 to 6, in combination with a semiconductor wafer or substrate (12), the contact pads being soldered (38) to the conductors (33) in alignment with the second holes (34).

8. A combination as claimed in claim 7, in combination with a connector block (14-17) having a multiplicity of connecting pins (46) secured therein, the connecting pins (46) passing into the first holes (42) and being soldered to the conductors (33).

9. An electronic circuit packaging member for interconnecting a ceramic substrate of the type having a multiple of electric connecting pads arranged about the periphery thereof, and a connector block arrangement of the type having a multiple of electric connecting pins arranged about the periphery of said ceramic substrate and spaced apart therefrom, said packaging member comprising a flat film of annular configuration having apertures near the inner periphery thereof registrable with said electric connecting pads and apertures near the outer periphery thereof registrable with said electric connecting pins, said film having conductive lands affixed thereto independent of each other, each of said lands being laid over one of said inner apertures and extending to a corresponding one of said outer apertures and having an aperture therein concentric with said outer aperture of said film, and one end of each of said lands

being soldered to an electric connecting pad and the other end being soldered to an electric connecting pin.

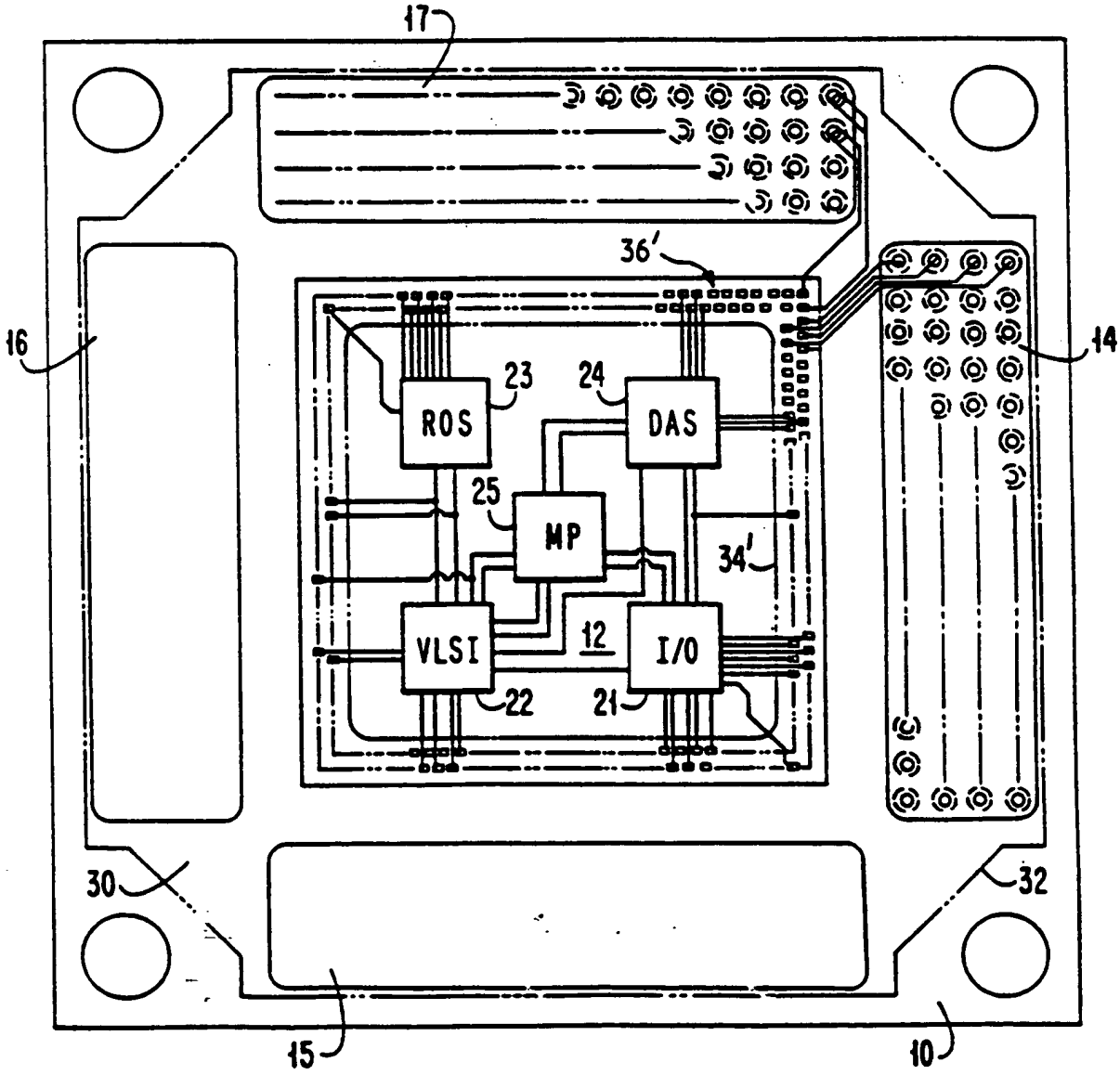

FIG. 1

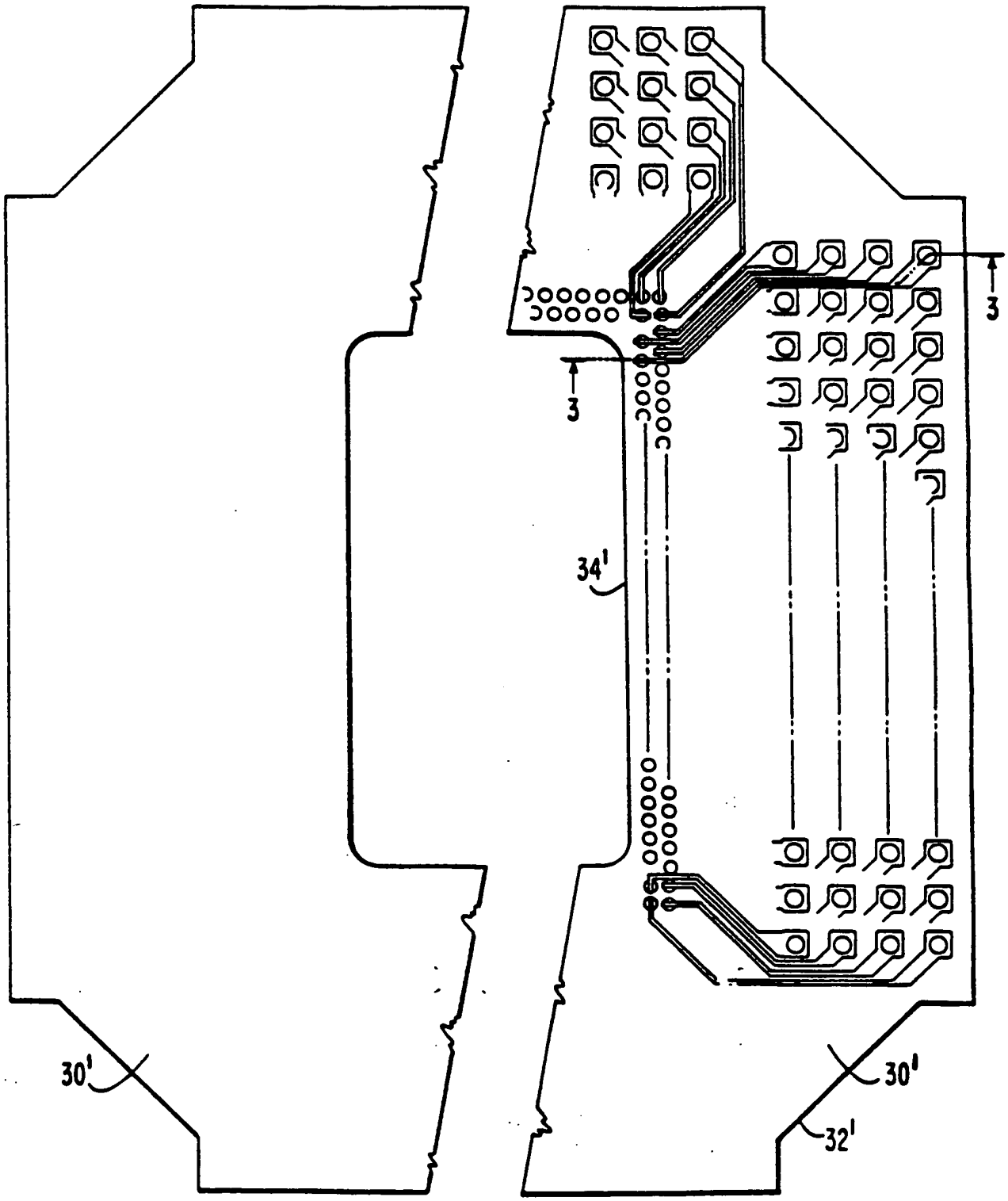

FIG. 2

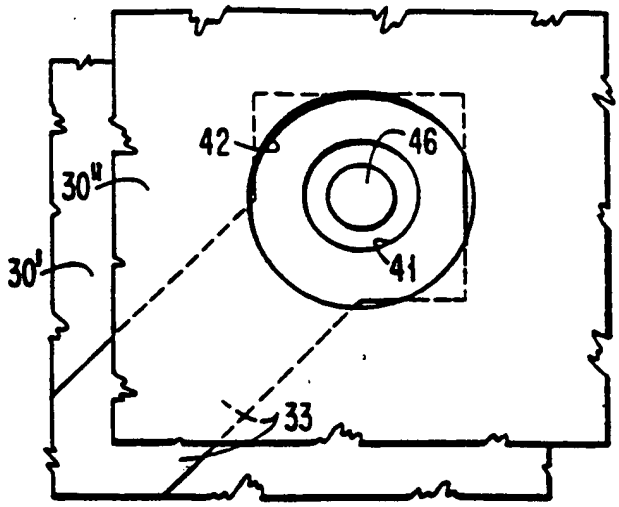

FIG. 5

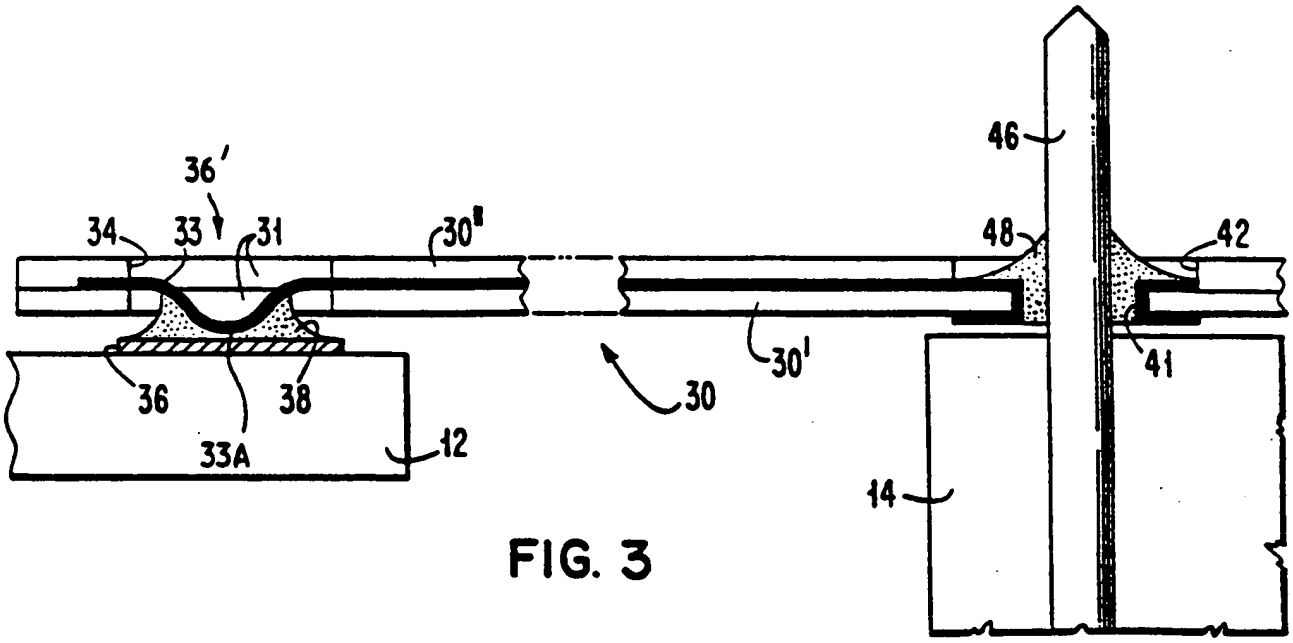

FIG. 3

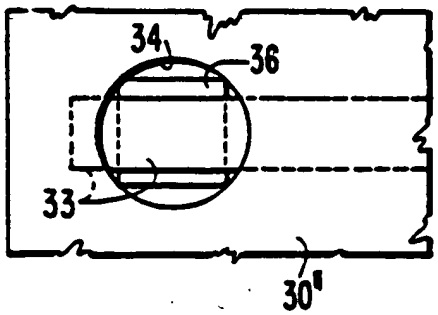

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application number: 0080041

EP 82 10 8766

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 3)
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 21, no. 6, November 6, 1978, NEW YORK (US). R.CECHANEK et al.:"Module package." Pages 2268-2269 * The whole document * ---	1,3, 7-9	H 01 L 23/48 H 01 L 23/52
A	US-A-3 662 230 (REDWANTZ) * Figure 6, column 5, lines 16-62 * ---	1,6,7, 9	
A	US-A-4 048 438 (ZIMMERMAN) * Figures 1,2,4; abstract * ---	2,9	
A	US-A-3 663 105 (SHAMASH et al.) * Figure 11; column 4, lines 42-63 * ---	4,5	TECHNICAL FIELDS SEARCHED (Int. Cl. 3) H 01 L
D,A	EP-A-0 013 562 (IBM) * Figure 1; abstract * -----	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18-01-1985	IRVINE R.J.

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